MODULE SPECIFICATION

Part 1: Information			
Module Title	Electronic Systems		
Module Code	UFMF7Q-30-3	Level	Level 6
For implementation from	2019-20		
UWE Credit Rating	30	ECTS Credit Rating	15
Faculty	Faculty of Environment & Technology	Field	Engineering, Design and Mathematics
Department	FET Dept of Engin Design & Mathematics		
Module type:	Standard		
Pre-requisites	None		
Excluded Combinations	None		
Co- requisites	None		
Module Entry requirements	None		

Part 2: Description

Educational Aims: This syllabus is designed to enable the learner to understand and design MOSIS and power electronic systems, as well as have an understanding of how VLSI circuits are used in industry.

Outline Syllabus: This module focusses on electronic design and power electronics, whilst also introducing the concepts of large scale integration. Key areas for study are electronic system design techniques and how to integrate these on a large scale within power electronics.

The topics covered in this unit are:
Electronic Design:
Sequential Design
Flip Flops
Mathematical Operators
Minimisation

Power Electronics:
Power Electronics Converters
Thyristor Controlled Series Compensator
Static VAR Compensator [SVC] / Static Synchronous Compensator (StatCom)

Unified Power Flow Controller [UPFC] / Dynamic Voltage Restoration [DVR]

Very Large-Scale Integration [VLSI]:
Component Construction
Metal Oxide Semiconductor Implementation Service (MOSIS)
Regular Array Structures
Analogue VLSI

Teaching and Learning Methods: See Assessment

Part 3: Assessment

Component A - Exam - 2 Hours - The assessment will encompass the analysis of power electronics systems and the creation of electronic sequences for given applications.

Component B - Individual Presentation – Students are given a sample electronic system and must produce and present an analysis of N and CMOS arrays with designs for a MOSIS logic device.

The resit assessment tasks for this module will involve a rework and reflective evaluation of the work carried out in the original task.

First Sit Components	**Final Assessment**	**Element weighting**	**Description**
Presentation - Component B		50 %	Individual presentation
Examination - Component A	✓	50 %	Examination (2 hours)
Resit Components	**Final Assessment**	**Element weighting**	**Description**
Presentation - Component B		50 %	Individual presentation
Examination - Component A	✓	50 %	Examination (2 hours)

Part 4: Teaching and Learning Methods

Learning Outcomes

On successful completion of this module students will achieve the following learning outcomes:

Module Learning Outcomes	Reference
Conduct power electronics analysis calculations	MO1
Create and evaluate electronic sequences for engineering applications.	MO2
Analyse NMOS and CMOS arrays for logic applications.	MO3
Design and evaluate MOSIS devices for logic applications.	MO4

Contact Hours

Independent Study Hours:	
Independent study/self-guided study	228
Total Independent Study Hours:	228
Scheduled Learning and Teaching Hours:	
Face-to-face learning	72
Total Scheduled Learning and Teaching Hours:	72
Hours to be allocated	300
Allocated Hours	300

Reading List

The reading list for this module can be accessed via the following link:

https://uwe.rl.talis.com/index.html

Part 5: Contributes Towards

This module contributes towards the following programmes of study: