MODULE SPECIFICATION

Part 1: Information			
Module Title	Digital Design 1		
Module Code	UFMFQK-15-2	Level	Level 5
For implementation from	2018-19		
UWE Credit Rating	15	ECTS Credit Rating	7.5
Faculty	Faculty of Environment & Technology	Field	Engineering, Design and Mathematics
Department	FET Dept of Engin Design & Mathematics		
Contributes towards			
Module type:	Standard		
Pre-requisites	Digital Principles 2018-19		
Excluded Combinations	None		
Co- requisites	None		
Module Entry requirements	None		

Part 2: Description
Overview: The module introduces an embedded system design for practical applications using logic design, hardware description languages (HDL) and logic synthesis tools. Students learn the principles of designing digital electronic circuits, with a focus on field programmable gate array (FPGA) implementation, including the tool flow, architecture, testing, and design for performance. The design and implementation of a functioning digital system with prototyping in FPGAs based on VHDL entry, using industry standard tools is the main focus of the module. **Educational Aims:** Students will develop technical skills to design, simulate, analyse and verify complex digital systems. The module will extend and further develop the practical, theoretical and professional skills needed for designing and implementing complex digital systems for a wide range of applications.

In addition to the learning outcomes, the educational experience may explore, develop, and practise but not formally discretely assess the following:

Working in multi-disciplinary teams,

Environmental and sustainability limitations in the life cycle of electronic products,

The use of creativity in developing innovative solutions to problems

Outline Syllabus: The syllabus includes:

Design, modelling and implementation of digital systems through the use of Hardware Description Languages (HDL) concepts, modelling techniques, hierarchical design, data path-controller models, hardware synthesis

VHDL modelling concepts, overview, language subsets for synthesis, Design Methodologies, State machines, Sequence enumeration, Use – Case models, Verification: tools and techniques, Synthesis: limitations, target architectures, tools

System-on-chip: trends, IP block, self-core processors

Teaching and Learning Methods: Accompanying lectures and tutorial sessions will present the formal aspects of the module. Students will be given small design problems to consider as part of their independent study in support of the lectures. These will then be discussed in tutorial sessions. Students will be expected to maintain an individual log book of both laboratory work and independent exercises as part of their professional development.

Part 3: Assessment

The module is assessed through two components. Each student is required to demonstrate competence in both theoretical and practical aspects of digital design through a two hour laboratory based examination.

Students develop the technical skills to design, simulate, analyse and verify a complex digital system through a collaborative learning strategy with the coursework involving a group work task. The output of the group work is a 15 page technical report and a group demonstration of their design.

Group work will be conducted under clear guidelines which provide for team members to allocate a weighting to each individual's contribution.

Assessments will be conducted in line with the SEEC guidelines for the level in conjunction with the discipline specific outcomes listed and referenced from the IET Handbook of Learning Outcomes for Accredited Programmes. Where a learning outcome is assessed more than once this is in both an individual and a group context.

Formative assessment will be provided through verbal feedback during laboratory sessions and through tutorial exercises. Ongoing feedback will also be provided to teams during the group work as part of the problem based learning exercise.

An initial set of structured laboratory exercises will extend the students understanding of the tools and techniques required, followed by a problem based team exercise. These exercises will provide the basis for the assessed coursework and for the laboratory exams.

First Sit Components	**Final Assessment**	**Element weighting**	**Description**
Group work - Component B	✓	50 %	Group project, report and demonstration
Examination - Component A		50 %	Laboratory examination (in-class) (2 hours)

Resit Components	Final Assessment	Element weighting	Description
Set Exercise - Component B	✓	50 %	Individual project, report (resubmission in light of feedback comments) and demonstration
Examination - Component A		50 %	Laboratory exam (in-class) (2 hours)

Part 4: Teaching and Learning Methods

Learning Outcomes

On successful completion of this module students will be able to:

	Module Learning Outcomes
MO1	Design microprocessor structures that demonstrate an understanding of digital engineering principles
MO2	Model the components in digital circuits to analyse both circuit and logic behaviour
MO3	Determine the performance, speed, area and power consumption of digital systems
MO4	Apply quantitative methods and computer software relevant to digital systems engineering
MO5	Demonstrate proficiency in the use of: High speed oscilloscopes and logic analysers, Microcomputer development tools, Digital CAD tools, including programmable components
MO6	Extract, search and interpret technical documentation

Contact Hours

Contact Hours	
Independent Study Hours:	
Independent study/self-guided study	114
Total Independent Study Hours:	114
Scheduled Learning and Teaching Hours:	
Face-to-face learning	36
Total Scheduled Learning and Teaching Hours:	36
Hours to be allocated	150
Allocated Hours	150

Reading List

The reading list for this module can be accessed via the following link:

https://uwe.rl.talis.com/modules/ufmfqk-15-2.html