Module Specification

Digital Design

Version: 2023-24, v3.0, 15 Mar 2023

Contents

Part 1: Information

Module title: Digital Design

Module code: UFMFE8-30-2

Level: Level 5

For implementation from: 2023-24

UWE credit rating: 30

ECTS credit rating: 15

Faculty: Faculty of Environment & Technology

Department: FET Dept of Engineering Design & Mathematics

Partner institutions: None

Field: Engineering, Design and Mathematics

Module type: Module

Pre-requisites: Digital Principles 2023-24

Excluded combinations: None

Co-requisites: None

Continuing professional development: No

Professional, statutory or regulatory body requirements: None

Part 2: Description

Overview: Not applicable

Features: Not applicable

Educational aims: In addition to the assessed Learning Outcomes, the educational experience may explore, develop, and practise but not formally discretely assess the following:

Working in multi-disciplinary teams

Environmental and sustainability limitations in the life cycle of electronic products

The use of creativity in developing innovative solutions to problems

Outline syllabus: Design, modelling and implementation of digital systems through the use of Hardware Description Languages (HDL):

Concepts, modelling techniques, hierarchical design, datapath-controller models, hardware synthesis.

Microprocessor architectures from a hardware design perspective, the basic components and functionality

Abstract RTL descriptions, Concrete RTL descriptions

Designers view v Programmers view

Internal components eg

Adders/subtracters, multipliers,

Registers,

Interrupts, I/O controllers

Control unit design,

Hardwired, Micro-coded, pipelined

High Level models

HDL:

Modelling concepts, overview, Language subsets for synthesis, Design Methodologies; ASM diagrams, Sequence enumeration, Use – Case models

Verification; Tools and techniques,

Synthesis; Limitations, target architectures, tools

System on Chip:

Design at the system level; Ip blocks, soft-core processors, interfaces

Real world issues; PCB design issues, power, reset

DSP hardware

Part 3: Teaching and learning methods

Teaching and learning methods: This module will extend and further develop the practical, theoretical and professional skills needed for designing and implementing complex digital systems for a wide range of applications.

An initial set of structured laboratory exercises will extend the students understanding of the tools and techniques required, followed by a problem based team exercise.

These exercises will provide the basis for the assessed coursework and for the laboratory exams. Students will be expected to maintain an individual log book of both laboratory work and independent exercises as part of their professional development.

Scheduled Learning in the form of lectures, tutorials, demonstrations and laboratory work will comprise 1/3 of the total study time.

Independent Learning will include directed reading, tutorial exercises, general reading of trade journals, academic papers and other texts.

Module Learning outcomes: On successful completion of this module students will achieve the following learning outcomes.

MO1 Demonstrate an understanding of digital engineering principles through the design of microprocessor and DSP structures. (E1)

MO2 Model the components in digital circuits to analyse both circuit and logic behaviour (E2)

MO3 Determine the performance, speed, area and power consumption of digital systems (E2)

MO4 Demonstrate the ability to apply quantitative methods and computer software relevant to digital systems engineering (E3)

MO5 Solve engineering problems through the use of schematic entry, hierarchy, hardware description, and finite state design tools to represent a complex digital design (E3)

MO6 Design and implement verification plans for simulation at the functional and timing level to verify the correct working of a digital design. (D6)

MO7 Demonstrate proficiency in the use of: High speed oscilloscopes and logic analysers , Microcomputer development tools, Digital CAD tools, including programmable components (P1, P2)

MO8 Show familiarity in obtaining, searching and interpreting technical documentation. (P4)

MO9 Show an understanding of intellectual property rights, industry codes of practice and standards in the design and development of digital systems. (P5, P6)

Hours to be allocated: 300

Contact hours:

Independent study/self-guided study = 228 hours

Face-to-face learning = 72 hours

Total = 300

Reading list: The reading list for this module can be accessed at readinglists.uwe.ac.uk via the following link https://uwe.rl.talis.com/modules/ufmfe8-30-2.html

Part 4: Assessment

Assessment strategy: Summative assessment is composed of group lab report and a presentation A maximum of three students will be allowed in a group for the Project and students are expected submit a 10-page report containing text, figures and references (UWE Harvard style). Individual student contribution will be assessed during the presentation. The spread of assessment is designed to ensure that the student demonstrates competence in both theoretical and practical aspects of the module. It also assesses the student's abilities as an individual (within a team setting) and in team work.

Formative assessment will be provided through verbal feedback during laboratory sessions and through tutorial exercises. Ongoing feedback will also be provided to teams during the group work as part of the problem based learning exercise.

Assessment tasks:

Presentation (First Sit)
Description: Presentation that includes a hardware or software demonstration of the work carried out in the Project assessment. Marking will be carried out for each student in the group.
Weighting: 25 %
Final assessment: Yes
Group work: Yes
Learning outcomes tested: MO2, MO6

Project (First Sit)

Description: Group design, report and demonstration. There can be maximum three students per group.
Weighting: 75 %
Final assessment: No
Group work: Yes
Learning outcomes tested: MO1, MO3, MO4, MO5, MO6, MO7, MO9

Presentation (Resit)
Description: Group Presentation that includes a hardware or software demonstration of the work carried out in the Project assessment. Marking will be carried out for each student in the group.
Weighting: 25 %
Final assessment: Yes
Group work: Yes
Learning outcomes tested: MO2, MO6

Project (Resit)
Description: Group design, report and demonstration. There can be maximum three students per group. (max. 10 pages)
Weighting: 75 %
Final assessment: No
Group work: Yes
Learning outcomes tested: MO1, MO3, MO4, MO5, MO6, MO7, MO9

Part 5: Contributes towards

This module contributes towards the following programmes of study:

Electrical and Electronic Engineering [AustonSingapore] BEng (Hons) 2023-24

Electronics and Telecommunication Engineering {Foundation} [Feb][FT][GCET][4yrs] BEng (Hons) 2021-22

Electronics and Telecommunication Engineering {Foundation} [Oct][FT][GCET][4yrs] BEng (Hons) 2021-22