MODULE SPECIFICATION

Part 1: Information			
Module Title	Digital Design		
Module Code	UFMFE8-30-2	Level	Level 5
For implementation from	2019-20		
UWE Credit Rating	30	ECTS Credit Rating	15
Faculty	Faculty of Environment & Technology	Field	Engineering, Design and Mathematics
Department	FET Dept of Engin Design & Mathematics		
Module type:	Standard		
Pre-requisites	Digital Principles 2019-20		
Excluded Combinations	None		
Co- requisites	None		
Module Entry requirements	None		

Part 2: Description

Educational Aims: In addition to the assessed Learning Outcomes, the educational experience may explore, develop, and practise but not formally discretely assess the following:

Working in multi-disciplinary teams

Environmental and sustainability limitations in the life cycle of electronic products

The use of creativity in developing innovative solutions to problems

Outline Syllabus: Design, modelling and implementation of digital systems through the use of Hardware Description Languages (HDL):

Concepts, modelling techniques, hierarchical design, datapath-controller models, hardware synthesis.

Microprocessor architectures from a hardware design perspective, the basic components and functionality

Abstract RTL descriptions, Concrete RTL descriptions

Designers view v Programmers view

Internal components eg

Adders/subtracters, multipliers,

Registers,

Interrupts, I/O controllers

Control unit design,

Hardwired, Micro-coded, pipelined

High Level models

HDL:

Modelling concepts, overview, Language subsets for synthesis, Design Methodologies; ASM diagrams, Sequence enumeration, Use – Case models

Verification; Tools and techniques,

Synthesis; Limitations, target architectures, tools

System on Chip:

Design at the system level; Ip blocks, soft-core processors, interfaces

Real world issues; PCB design issues, power, reset

DSP hardware

Teaching and Learning Methods: This module will extend and further develop the practical, theoretical and professional skills needed for designing and implementing complex digital systems for a wide range of applications.

An initial set of structured laboratory exercises will extend the students understanding of the tools and techniques required, followed by a problem based team exercise.

These exercises will provide the basis for the assessed coursework and for the laboratory exams. Students will be expected to maintain an individual log book of both laboratory work and independent exercises as part of their professional development.

Scheduled Learning in the form of lectures, tutorials, demonstrations and laboratory work will comprise 1/3 of the total study time.

Independent Learning will include directed reading, tutorial exercises, general reading of trade journals, academic papers and other texts.

Part 3: Assessment
Summative assessment is composed of one in-class laboratory exercise under controlled conditions, an individual lab report and a group exercise. The spread of assessment is designed to ensure that the student demonstrates competence in both theoretical and practical aspects of the module. It also assesses their abilities as an individual and in team work. Formative assessment will be provided through verbal feedback during laboratory sessions and through tutorial exercises. Ongoing feedback will also be provided to teams during the group work as part of the problem based learning exercise.

First Sit Components	Final Assessment	Element weighting	Description
Report - Component B		12.5 %	Individual lab report
Project - Component B	✓	37.5 %	Group design, report and demonstration
Examination - Component A		50 %	Laboratory exam
Resit Components	**Final Assessment**	**Element weighting**	**Description**
Final Project - Component B	✓	50 %	Individual design, report & demonstration
Examination - Component A		50 %	Laboratory exam

Part 4: Teaching and Learning Methods

Learning Outcomes

On successful completion of this module students will achieve the following learning outcomes:

Module Learning Outcomes	Reference
Demonstrate an understanding of digital engineering principles through the design of microprocessor and DSP structures. (E1)	MO1
Model the components in digital circuits to analyse both circuit and logic behaviour (E2)	MO2
Determine the performance, speed, area and power consumption of digital systems (E2)	MO3
Demonstrate the ability to apply quantitative methods and computer software relevant to digital systems engineering (E3)	MO4
Solve engineering problems through the use of schematic entry, hierarchy, hardware description, and finite state design tools to represent a complex digital design (E3)	MO5
Design and implement verification plans for simulation at the functional and timing level to verify the correct working of a digital design. (D6)	MO6
Demonstrate proficiency in the use of: High speed oscilloscopes and logic analysers , Microcomputer development tools, Digital CAD tools, including programmable components (P1, P2)	MO7
Show familiarity in obtaining, searching and interpreting technical documentation. (P4)	MO8
Show an understanding of intellectual property rights, industry codes of practice and standards in the design and development of digital systems. (P5, P6)	MO9

Contact Hours

Independent Study Hours:

Independent study/self-guided study	228
Total Independent Study Hours:	228

Scheduled Learning and Teaching Hours:

	Face-to-face learning	72
	Total Scheduled Learning and Teaching Hours:	72
	Hours to be allocated	300
	Allocated Hours	300
Reading List	*The reading list for this module can be accessed via the following link:* https://uwe.rl.talis.com/modules/ufmfe8-30-2.html	

Part 5: Contributes Towards

This module contributes towards the following programmes of study:

Electrical and Electronic Engineering {Top-Up} [Feb][FT][AustonSingapore][1yr] BEng (Hons) 2019-20
Electrical and Electronic Engineering {Top-Up} [May][PT][AustonSingapore][1.3yrs] BEng (Hons) 2019-20
Electrical and Electronic Engineering {Top-Up} [Feb][PT][AustonSingapore][1.3yrs] BEng (Hons) 2019-20
Electrical and Electronic Engineering {Top-Up} [Oct][PT][AustonSingapore][1.3yrs] BEng (Hons) 2019-20
Electrical and Electronic Engineering {Top-Up} [Oct][PT][AustonSriLanka][1.3yrs] BEng (Hons) 2019-20
Electrical and Electronic Engineering {Top-Up} [Feb][PT][AustonSriLanka][1.3yrs] BEng (Hons) 2019-20
Electrical and Electronic Engineering {Top-Up} [May][PT][AustonSriLanka][1.3yrs] BEng (Hons) 2019-20
Electrical and Electronic Engineering {Top-Up} [Feb][FT][AustonSriLanka][1yr] BEng (Hons) 2019-20
Electrical and Electronic Engineering {Top-Up} [May][FT][AustonSingapore][1yr] BEng (Hons) 2019-20
Electrical and Electronic Engineering {Top-Up} [May][FT][AustonSriLanka][1yr] BEng (Hons) 2019-20
Electrical and Electronic Engineering {Top-Up} [Oct][FT][AustonSriLanka][1yr] BEng (Hons) 2019-20
Electrical and Electronic Engineering {Top-Up} [Oct][FT][[AustonSingapore][1yr] BEng (Hons) 2019-20
Electronic and Computer Engineering [Sep][FT][Frenchay][3yrs] BEng (Hons) 2018-19
Electronic and Computer Engineering [Sep][SW][Frenchay][4yrs] BEng (Hons) 2018-19
Electronic and Computer Engineering {Top Up} [Aug][FT][SHAPE][1yr] BEng (Hons) 2018-19
Electronic and Computer Engineering {Top Up} [Aug][PT][SHAPE][2yrs] BEng (Hons) 2018-19
Electronic and Computer Engineering [Sep][PT][GlosColl][5yrs] BEng (Hons) 2018-19
Electronic and Computer Engineering {Apprenticeship} [Sep][PT][GlosColl][5yrs] BEng (Hons) 2018-19
Electrical and Electronic Engineering [Sep][SW][Northshore][5yrs] MEng 2018-19
Electrical and Electronic Engineering [Sep][SW][Frenchay][5yrs] MEng 2018-19