MODULE SPECIFICATION

Part 1: Information			
Module Title	Digital Principles		
Module Code	UFMFF8-30-1	Level	Level 4
For implementation from	2018-19		
UWE Credit Rating	30	ECTS Credit Rating	15
Faculty	Faculty of Environment & Technology	Field	Engineering, Design and Mathematics
Department	FET Dept of Engin Design & Mathematics		
Contributes towards	Electronic Engineering [Sep][SW][Frenchay][5yrs] MEng 2018-19 Electrical and Electronic Engineering [Sep][SW][Northshore][5yrs] MEng 2018-19 Electronic and Computer Engineering [Sep][FT][Frenchay][3yrs] BEng (Hons) 2018-19 Electrical and Electronic Engineering [Sep][SW][Frenchay][5yrs] MEng 2018-19 Electronic and Computer Engineering [Sep][SW][Frenchay][4yrs] BEng (Hons) 2018-19 Electronic and Computer Engineering {Top Up} [Aug][FT][SHAPE][1yr] BEng (Hons) 2018-19 Electronic and Computer Engineering {Top Up} [Aug][PT][SHAPE][2yrs] BEng (Hons) 2018-19 Electronic and Computer Engineering [Sep][PT][GlosColl][5yrs] BEng (Hons) 2018-19 Electronic and Computer Engineering {Apprenticeship} [Sep][PT][GlosColl][5yrs] BEng (Hons) 2018-19		
Module type:	Standard		
Pre-requisites	None		
Excluded Combinations	None		
Co- requisites	None		
Module Entry requirements	None		

Part 2: Description

Educational Aims: In addition to the Learning Outcomes, the educational experience may explore, develop, and practise but not formally discretely assess the following:
Develop competence in problem identification, analysis, design and implementation (D4, D6).
Understanding of the need for a high level of professional and ethical conduct (S5).

Outline Syllabus: Combinational Logic:

Number systems (decimal, binary, Hexadecimal, conversion, 1's complement and 2's complement representations).

Combinational logic design principles (Truth tables, Basic Logic gates (AND, OR, XOR, NAND, NOR, NOT), Boolean algebra, circuit analysis, circuit synthesis), Basic characteristics of digital ICs.

Minimisation (from Venn diagrams to 2D maps, Karnaugh maps, the Quine-McCluskey algoritms, don't care in Karnaugh maps).

Static and dynamic hazards.

Implementation using discrete gates, multiplexers, ROMs, PLAs, PLDs, CPLDs, FPGAs.

Sequential Logic:

Basic latches and flip-flops (RS, D, JK), clocking and evolution of flip-flops.

Counters (synchronous counters, up-down counters, analysing synchronous counters).

Shift registers (serial in parallel out, cyclic, pseudorandom sequence generator).

Finite state machines, State diagrams, tables and equations.

State reduction. Structured state assignment. Incompletely specified state tables.

Design process of synchronous sequential circuits.

Implementation using decoders, multiplexers and programmable devices.

Introduction to VHDL:

Setting the context.

Design flow for hardware description languages (capture, implementation, functional simulation, timing simulation, hardware verification).

VHDL structure (interface, implementations and components).

Design approaches in VHDL.

Microcontrollers:

Review of the design flow in micro-controllers based applications.

Review of basic functional parts a microcontroller, including internal architecture, programming model, op-codes, addressing modes, memory mapping and address decoding.

Use of digital electronics CAD tools, and simple system simulations.

Design and implementation of single-chip microcontroller-based embedded system.

Simple assembly language and high-level language software design and implementation.

Teaching and Learning Methods: While the first part of the module covers the basic principles of digital systems, the second part covers the basic principles of micro-controllers and related development environments. The theoretical concepts are formally introduced in lectures. These are supported by directed reading and well detailed worked examples. The practical content exposes the students to the practical aspect of the module. The laboratory exercises complement the theoretical aspect of the module. In the first semester, the lab activity involves the familiarisation with an integrated development environment (IDE). The real time implementation focuses on an FPGA hardware platform. In relation to the second semester, the entire detailed syllabus is addressed in the context of specific devices and development environments to be used in the laboratory work, as exemplars of the more generic issues. Students will gain hands-on knowledge in an experimental project-based environment. Relevant ethical issues will be highlighted and students will be encouraged to consider these further through directed reading.

Approximate time in hours
Contact: 72
Assimilation and skill development: 140
Undertaking coursework: 40
Exam preparation: 48
Total: 300

Part 3: Assessment

A formal exam that contributes 50% towards the final mark of the module. The examination is summative and assesses the students' understanding of concepts and techniques, and their ability to apply them in relatively straightforward problems.

A coursework that contributes 50% towards the final mark of the module. The coursework consists of a logbook (40%) and a small scale lab project (60%).

Formative assessment will be provided as oral feedback throughout the laboratory sessions particularly with respect to the lab exercises and the log-book entries.

First Sit Components	**Final Assessment**	**Element weighting**	**Description**
Set Exercise - Component B		20 %	Logbook
Project - Component B		30 %	Small scale lab project
Examination - Component A	✓	50 %	Exam (180 minutes)
Resit Components	**Final Assessment**	**Element weighting**	**Description**
Written Assignment - Component B		50 %	Coursework
Examination - Component A	✓	50 %	

Part 4: Teaching and Learning Methods

Learning Outcomes

On successful completion of this module students will be able to:

	Module Learning Outcomes
MO1	Knowledge and understanding of the basic mathematical principles as applied to the description and analysis of digital systems (US2)
MO2	An understanding of engineering principles as applied to digital systems and the ability to assess their performances (E1, E2)
MO3	An understanding of and an ability to apply top-down digital design methods in the synthesis of digital systems (E4)
MO4	The ability to use integrated development environments to describe, simulate, implement and verify the correctness of digital designs (E3)
MO5	Competence in using specific Electronic Design Automation tools (P1)
MO6	An understanding of basic microcontroller structure and internal architecture (E1)
MO7	The ability to understand and use development tools to design, program, implement and test example applications (E3)
MO8	Competence in using technical literature and the ability to obtain documentation from various sources (P4)

Contact Hours

Contact Hours	
Independent Study Hours:	
Independent study/self-guided study	228
Total Independent Study Hours:	228
Scheduled Learning and Teaching Hours:	
Face-to-face learning	72
Total Scheduled Learning and Teaching Hours:	72
Hours to be allocated	300
Allocated Hours	300

Reading List

The reading list for this module can be accessed via the following link:

https://uwe.rl.talis.com/modules/ufmff8-30-1.html