Module Specification

System Design Using HDLs

Version: 2025-26, v4.0, Approved

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Part 1: Information

Module title: System Design Using HDLs

Module code: UFME7G-15-M

Level: Level 7

For implementation from: 2025-26

UWE credit rating: 15

ECTS credit rating: 7.5

College: College of Arts, Technology and Environment

School: CATE School of Engineering

Partner institutions: None

Field: Engineering, Design and Mathematics

Module type: Module

Pre-requisites: None

Excluded combinations: None

Co-requisites: None

Continuing professional development: No

Professional, statutory or regulatory body requirements: None

Part 2: Description

Overview: This module teaches concepts of HDLs to design digital systems, HDL on programmable devices such as CPLD and FPGA, write HDL codes for simple and complex systems and implement HDL codes on FPGA hardware. It also covers VHDL, in the design process with the help of examples. Many digital system design examples, ranging in complexity from a simple binary adder to a microprocessor, are taught in this module.

In addition, the module emphasis on providing understanding of VHDL in the digital design process using the basic and necessary features for digital design systems.

Features: Understanding of use of VHDL in co-design digital systems
Awareness of chip design tools and techniques
Knowledge of safety standard for hardware system design

Educational aims: This module is a mandatory and teaches how to design digital systems using VHDL on FPGA hardware. The module becomes essential part of the programme curriculum and is of important use in telecommunication engineering, devices and systems.

Outline syllabus: Comparison with other HDLs
Role of VHDL in hardware-software co-design
Simulation and Verification
Design for synthesis and re-use
FPGAs as target hardware
System-on-chip design tools and techniques
Safety standards for hardware systems, eg IEC61508

Part 3: Teaching and learning methods

Teaching and learning methods: Scheduled Learning in the form of lectures, tutorials, demonstrations and independent learning laboratory work. The lectures will covers the basic and advanced concepts in designing novel digital systems and the lab work will be used to demonstrate the practical skills by implementing the conceptual understanding. A series of lab/tutorial tasks will help the students to learn system design individually as well as with in the group. The feedback on the students lab work will prepare students to complete the final project report and its demonstration.

Independent Learning will include directed reading, tutorial exercises, general reading of trade journals, academic papers and other texts.

Module Learning outcomes: On successful completion of this module students will achieve the following learning outcomes.

MO1 Demonstrate a cognitive skill to design and develop a new digital system by using HDLs, VHDL, appropriate verification and debug tools and methods.

MO2 Ability to evaluate the new digital systems considering the commercial risks, constraints while solving the systems problems in uncertain situations.

Hours to be allocated: 150

Contact hours:

Independent study/self-guided study = 126 hours

Face-to-face learning = 24 hours

Reading list: The reading list for this module can be accessed at readinglists.uwe.ac.uk via the following link https://uwe.rl.talis.com/modules/ufme7g-15-m.html

Part 4: Assessment

Assessment strategy: The module will be assessed as follows:

The students will require to write a report which will assess the student's ability to develop a solution to a design specification along with their understanding of the design principles necessary. The students will be working in groups and will submit a written report to demonstrate design skills and also to explain verbally innovative solution to a design problem.

Formative feedback will be provided during the laboratory sessions and tutorials.

Resit is the same as the first sit

Assessment tasks:

Report (First Sit)

Description: Written final project report will assess the design and development of a new digital system by using HDLs, VHDL, appropriate verification and debug tools and methods.
Weighting: 100 %
Final assessment: Yes
Group work: Yes
Learning outcomes tested: MO1, MO2

Report (Resit)
Description: Written final project report will assess the design and development of a new digital system by using HDLs, VHDL, appropriate verification and debug tools and methods.
Weighting: 100 %
Final assessment: Yes
Group work: Yes
Learning outcomes tested: MO1, MO2

Part 5: Contributes towards

This module contributes towards the following programmes of study:

Electronics and Telecommunication Engineering [GCET] MSc 2025-26

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Electronic Engineering [Sep][SW][Frenchay][5yrs] - Withdrawn MEng 2021-22