Module Specification

Digital System Design

Version: 2025-26, v3.0, 23 Apr 2025

Contents

Part 1: Information

Module title: Digital System Design

Module code: UFMFQT-15-2

Level: Level 5

For implementation from: 2025-26

UWE credit rating: 15

ECTS credit rating: 7.5

College: College of Arts, Technology and Environment

School: CATE School of Engineering

Partner institutions: None

Field: Engineering, Design and Mathematics

Module type: Module

Pre-requisites: Applied Electronics 2024-25

Excluded combinations: None

Co-requisites: None

Continuing professional development: No

Professional, statutory or regulatory body requirements: None

Part 2: Description

Overview: This module introduces a systematic way of designing complex digital electronic systems (not circuits) such as microprocessors, network routers using hardware description languages (HDL) and logic synthesis tools. Students will develop technical skills to design, simulate, analyse and verify complex digital systems. Students learn the principles of designing digital electronic circuits, with a focus on field programmable gate array (FPGA) implementation, including the tool flow, architecture, testing, and design for performance.

The design and implementation of a functioning digital system with prototyping in FPGAs based on HDL entry, using industry standard tools is the main focus of the module. The module will extend and further develop the practical, theoretical and professional skills needed for designing and implementing complex digital systems for a wide range of applications.

Features: Not applicable

Educational aims: This module aims to develop the students' understanding in digital design from the electronics knowledge gained at level 4.
The module introduces low-level coding and hardware design.

Outline syllabus: Hardware Description Languages
Digital Logic Circuit modelling concepts
Design Methodologies
Language subsets for synthesis
Finite State Machines
Verification: tools and techniques
Synthesis: limitations, target architecture, tools
Digital Electronic Systems
Datapath and Controller Design
Systems-on-chip
Trends, IP blocks, softcore processors

Part 3: Teaching and learning methods

Teaching and learning methods: The delivery is intended to ensure that students have opportunity to develop practical lab-based skills alongside theoretical understanding of digital design principles through integrated theory and laboratory sessions.

Module Learning outcomes: On successful completion of this module students will achieve the following learning outcomes.

MO1 Design, simulate, and implement complex digital designs using EDA tools.

MO2 Analyse complex digital designs using EDA tools and laboratory equipment.

Hours to be allocated: 150

Contact hours:

Independent study/self-guided study = 114 hours

Face-to-face learning = 36 hours

Reading list: The reading list for this module can be accessed at readinglists.uwe.ac.uk via the following link https://rl.talis.com/3/uwe/lists/F6751359-FFFC-EBE0-301C-135ECBB95D45.html?lang=en-GB&login=1

Part 4: Assessment

Assessment strategy: In this module students individually develop the technical skills to design, simulate, analyse and verify a complex digital system through a collaborative learning strategy with the aid of a set of structured laboratory exercises. This will extend the students understanding of the tools and techniques required to become an expert in digital system design.

Assessment of this module consists of a portfolio of regular laboratory assignments of increasing complexity and scope. The final milestone hereby provides the summative assessment, while the earlier milestones provided immediate feedback.

Resit is same as first sit

Assessment tasks:

Portfolio (First Sit)
Description: Portfolio (4 intermediate milestones, 1 final milestone, totalling app. 50 pages including source code and simulation)
Weighting: 100 %
Final assessment: Yes
Group work: No

Learning outcomes tested: MO1, MO2

Portfolio (Resit)
Description: Portfolio (4 intermediate milestones, 1 final milestone, totalling app. 50 pages including source code and simulation)
Weighting: 100 %
Final assessment: Yes
Group work: No
Learning outcomes tested: MO1, MO2

Part 5: Contributes towards

This module contributes towards the following programmes of study:

Electronic Engineering [Frenchay] WITHDRAWN BEng (Hons) 2023-24

Electronic Engineering {Foundation} [Frenchay] WITHDRAWN BEng (Hons) 2023-24

Electronic and Computer Engineering {Apprenticeship-GLOSCOLL} [GlosColl] BEng (Hons) 2023-24

Electronic and Computer Engineering [GlosColl] BEng (Hons) 2023-24

Electronic and Computer Engineering [Frenchay] BEng (Hons) 2024-25

Electronic and Computer Engineering [Frenchay] BEng (Hons) 2024-25

Electronic and Computer Engineering [GlosColl] BEng (Hons) 2023-24

Electronic and Computer Engineering {Apprenticeship-GLOSCOLL} [GlosColl] BEng (Hons) 2023-24