Module Specification

Introduction to CMOS IC Design

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Part 1: Information

Module title: Introduction to CMOS IC Design

Module code: UFMFPR-15-3

Level: Level 6

For implementation from: 2024-25

UWE credit rating: 15

ECTS credit rating: 7.5

College: College of Arts, Technology and Environment

School: CATE School of Engineering

Partner institutions: None

Field:

Module type: Standard

Pre-requisites: None

Excluded combinations: None

Co-requisites: None

Continuing professional development: No

Professional, statutory or regulatory body requirements: None

Part 2: Description

Overview: This module teaches the conceptual and technological details of complementary metal oxide semiconductor (CMOS) IC design implementation. It covers fundamental principles of CMOS circuit design and performance analysis, as well as background knowledge of IC fabrication. Using the professional design kit of a state-of-the-art design environment, students will practice the analog IC design flow of schematic entry, design simulation, circuit layout with electrical static discharge (ESD) protection, and finally, generate IC fabrication files.

Features: Not applicable

Educational aims: This module provides students with skills and techniques in complementary metal oxide semiconductor (CMOS) IC design implementation. It covers fundamental principles of CMOS circuit design and performance analysis, as well as background knowledge of IC fabrication. Using the professional design kit of the Cadence design environment, students will practice the analog IC design flow of schematic entry, design simulation, circuit layout with electrical static discharge (ESD) protection, and finally, generate IC fabrication files.

Outline syllabus: 1. MOS device physics, CMOS analog circuit blocks (e.g. current mirror, differential pair), digital blocks and IC fabrication processing technology.
2. Analog IC design implementation using IC design CAD tool of Cadence for functional simulation and post-layout simulation, design rules for custom layout, and layout techniques.
3. Circuit protection, IC packaging.

Part 3: Teaching and learning methods

Teaching and learning methods: This module will run in a seminar-style: each 3-hour teaching session includes an hour teaching block followed by a 2-hour lab session where students will work independently mainly focusing on the completion of their assigned coursework.

Module Learning outcomes: On successful completion of this module students will achieve the following learning outcomes.

MO1 Demonstrate knowledge and understanding of MOS device physics, CMOS analog circuit blocks, and IC fabrication processing technology.

MO2 Be able to use a state-of-the-art IC design CAD tool suite and generate fabrication files

MO3 Demonstrate the understanding of circuit imperfection related performance deviation and be familiar with IC packaging.

MO4 Be able to design application-specific ICs for power/size restricted applications

Hours to be allocated: 150

Contact hours:

Independent study/self-guided study = 102 hours

Lectures = 48 hours

Total = 150

Reading list: The reading list for this module can be accessed at readinglists.uwe.ac.uk via the following link https://rl.talis.com/3/uwe/lists/D13B8AD0-DBCC-9629-8B68-3933773ACAE9.html?lang=en&login=1

Part 4: Assessment

Assessment strategy: This module is assessed by the individual coursework + live demonstration, and presentation. 25% weighting is allocated to the presentation, and 75% weighting is allocated to the submitted materials and live demonstration of the project. Progress in Lab sessions will be recorded as the backup for the unlikely cases affecting the live demonstration, such as potential computer network issues.

The coursework, released in the first teaching session, is to implement a low-power active contactless electrode for physiological measurements in a 0.35 μm CMOS process.

The submission of IC design documents for the coursework assignment should include the schematic design, simulated results (gain-bandwidth, input inferred noise, CMRR, and power consumption), circuit layout with circuits protection, and final IC fabrication files.

The coursework report will be submitted by the end of the term followed by a live demonstration.

Assessment tasks:

Presentation (First Sit)
Description: 15 minutes presentation (including 5 minutes questions and answers) and 5 minutes live-demonstration of the project
Weighting: 25 %
Final assessment: No
Group work: No
Learning outcomes tested: MO1, MO3

Project (First Sit)
Description: The coursework, released in the first teaching session, is to implement a low-power active contactless electrode for physiological measurements in a 0.35 µm CMOS process.
Weighting: 75 %
Final assessment: Yes
Group work: No
Learning outcomes tested: MO2, MO4

Presentation (Resit)
Description: 15 minutes presentation (including 5 minutes questions and answers) and 5 minutes live-demonstration of the project
Weighting: 25 %
Final assessment: No
Group work: No
Learning outcomes tested: MO1, MO3

Project (Resit)
Description: The coursework, released in the first teaching session, is to implement a low-power active contactless electrode for physiological measurements in a 0.35 µm CMOS process.

Weighting: 75 %

Final assessment: Yes

Group work: No

Learning outcomes tested: MO2, MO4

Part 5: Contributes towards

This module contributes towards the following programmes of study: