Module Specification

Introduction to Digital Design

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Contents

Part 1: Information

Module title: Introduction to Digital Design

Module code: UFME49-15-0

Level: Level 3

For implementation from: 2022-23

UWE credit rating: 15

ECTS credit rating: 7.5

Faculty: Faculty of Environment & Technology

Department: FET Dept of Engineering Design & Mathematics

Partner institutions: Global College of Engineering and Technology (GCET)

Delivery locations: Global College of Engineering and Technology (GCET)

Field: Engineering, Design and Mathematics

Module type: Standard

Pre-requisites: None

Excluded combinations: None

Co-requisites: None

Continuing professional development: No

Professional, statutory or regulatory body requirements: None

Part 2: Description

Overview: Not applicable

Features: Not applicable

Educational aims: In addition to the Learning Outcomes, the educational experience may explore, develop, and practise but not formally discretely assess the following:

Develop competence in problem identification, analysis, design and implementation (D4, D6).
Understanding of the need for a high level of professional and ethical conduct (S5).

Outline syllabus: Combinational Logic:

Number systems (decimal, binary, Hexadecimal, conversion, 1's complement and 2's complement representations).

Combinational logic design principles (Truth tables, Basic Logic gates (AND, OR, XOR, NAND, NOR, NOT), Boolean algebra, circuit analysis, circuit synthesis), Basic characteristics of digital ICs.

Minimisation (from Venn diagrams to 2D maps, Karnaugh maps, the Quine-McCluskey algoritms, don't care in Karnaugh maps).

Static and dynamic hazards.

Implementation using discrete gates, multiplexers, ROMs, PLAs, PLDs, CPLDs, FPGAs.

Sequential Logic:

Basic latches and flip-flops (RS, D, JK), clocking and evolution of flip-flops.

Counters (synchronous counters, up-down counters, analysing synchronous counters).

Shift registers (serial in parallel out, cyclic, pseudorandom sequence generator).

Finite state machines, State diagrams, tables and equations.

State reduction. Structured state assignment. Incompletely specified state tables.

Design process of synchronous sequential circuits.

Implementation using decoders, multiplexers and programmable devices.

Introduction to VHDL:

Setting the context.

Design flow for hardware description languages (capture, implementation, functional simulation, timing simulation, hardware verification).

VHDL structure (interface, implementations and components).

Design approaches in VHDL.

Microcontrollers:

Review of the design flow in micro-controllers based applications.

Review of basic functional parts a microcontroller, including internal architecture, programming model, op-codes, addressing modes, memory mapping and address decoding.

Use of digital electronics CAD tools, and simple system simulations.

Design and implementation of single-chip microcontroller-based embedded system.

Simple assembly language and high-level language software design and implementation.

Part 3: Teaching and learning methods

Teaching and learning methods: While the first part of the module covers the basic principles of digital systems, the second part covers the basic principles of micro-controllers and related development environments. The theoretical concepts are formally introduced in lectures. These are supported by directed reading and well detailed worked examples. The practical content exposes the students to the practical aspect of the module. The laboratory exercises complement the theoretical aspect of the module. In the first semester, the lab activity involves the familiarisation with an integrated development environment (IDE). The real time implementation focuses on an FPGA hardware platform. In relation to the second semester, the entire detailed syllabus is addressed in the context of specific devices and development environments to be used in the laboratory work, as exemplars of the more generic issues. Students will gain hands-on knowledge in an experimental project-based environment. Relevant ethical issues will be highlighted and students will be encouraged to consider these further through directed reading.

Module Learning outcomes: On successful completion of this module students will achieve the following learning outcomes.

MO1 Apply basic mathematical principles to the description and analysis of digital systems (US2)

MO2 Implement the engineering principles for digital systems and develop the ability to assess their performances (E1, E2)

MO3 Effectively apply top-down digital design methods in the synthesis of digital systems (E4)

MO4 Evaluate basic microcontroller structure and internal architecture (E1)

MO5 Develop competence in using technical literature related to digital design and the ability to obtain relevant documentation from various sources (P4)

Hours to be allocated: 150

Contact hours:

Independent study/self-guided study = 114 hours

Face-to-face learning = 36 hours

Total = 150

Reading list: The reading list for this module can be accessed at readinglists.uwe.ac.uk via the following link https://uwe.rl.talis.com/modules/ufmff8-30-1.html

Part 4: Assessment

Assessment strategy: A presentation of the coursework described below contributes 25% towards the final mark of the module. It is summative and assesses the students' understanding of the key concepts and techniques explored as part of the practical work and the coursework, and their ability to apply thee to other relatively straightforward problems.

A coursework that contributes 75% towards the final mark of the module. The coursework consists of a logbook of practical work, exercises practiced during lab/practical hours and a small-scale lab project.

The referral work will be of 2 parts: (i) a presentation of the small-scale project done for the first sit contributing 25%, (ii) a logbook developed from the practical works extended with an essay to evaluate the practical works done including a self-reflection, which contributes 75 %.

Assessment components:

Presentation - Component A (First Sit)
Description: Presentation
Weighting: 25 %
Final assessment: Yes
Group work: No
Learning outcomes tested: MO1, MO2, MO3

Project - Component B (First Sit)
Description: The coursework consists of lab reports of two practical sessions and a small scale project report.

Weighting: 75 %

Final assessment: No

Group work: No

Learning outcomes tested: MO1, MO2, MO3, MO4, MO5

Presentation - Component A (Resit)

Description: Pre-recorded presentation

Weighting: 25 %

Final assessment: Yes

Group work: No

Learning outcomes tested: MO1, MO2, MO3

Written Assignment - Component B (Resit)

Description: The coursework consists of a small-scale project report.

Weighting: 75 %

Final assessment: No

Group work: No

Learning outcomes tested: MO1, MO2, MO3, MO4, MO5

Part 5: Contributes towards

This module contributes towards the following programmes of study:

Computer Science (Artificial Intelligence) {Foundation} [GCET] BSc (Hons) 2022-23

Computer Science (Smart Devices) {Foundation} [GCET] BSc (Hons) 2022-23

Computer Science {Foundation} [GCET] BSc (Hons) 2022-23

Computer Science {Foundation}[Oct][FT][GCET][4yrs] BSc (Hons) 2022-23