Module Specification

Digital System Design

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Part 1: Information

Module title: Digital System Design

Module code: UFMFQT-15-2

Level: Level 5

For implementation from: 2021-22

UWE credit rating: 15

ECTS credit rating: 7.5

Faculty: Faculty of Environment & Technology

Department: FET Dept of Engineering Design & Mathematics

Partner institutions: None

Delivery locations: Frenchay Campus

Field: Engineering, Design and Mathematics

Module type: Standard

Pre-requisites: None

Excluded combinations: None

Co-requisites: Applied Electronics 2021-22

Continuing professional development: No

Professional, statutory or regulatory body requirements: None

Part 2: Description

Overview: This module introduces a systematic way of designing complex digital electronic systems (not circuits) such as microprocessors, network routers using hardware description languages (HDL) and logic synthesis tools. Students will develop technical skills to design, simulate, analyse and verify complex digital systems. Students learn the principles of designing digital electronic circuits, with a focus on field programmable gate array (FPGA) implementation, including the tool

flow, architecture, testing, and design for performance.

The design and implementation of a functioning digital system with prototyping in FPGAs based on HDL entry, using industry standard tools is the main focus of the module. The module will extend and further develop the practical, theoretical and professional skills needed for designing and implementing complex digital systems for a wide range of applications.

Features: Not applicable

Educational aims: This module aims to develop the students' understanding in digital design from the electronics knowledge gained at level 4.
The module introduces low-level coding and hardware design.

Outline syllabus: Hardware Description Languages
Digital Logic Circuit modelling concepts
Design Methodologies
Language subsets for synthesis
Finite State Machines
Verification: tools and techniques
Synthesis: limitations, target architecture, tools
Digital Electronic Systems
Datapath and Controller Design
Systems-on-chip
Trends, IP blocks, softcore processors

Part 3: Teaching and learning methods

Teaching and learning methods: The delivery is intended to ensure that students have opportunity to develop practical lab-based skills alongside theoretical understanding of digital design principles through integrated theory and laboratory sessions.

Module Learning outcomes: On successful completion of this module students will achieve the following learning outcomes.

MO1 Demonstrate an understanding of digital circuit components and systems

MO2 Ability to model the components in digital electronic systems using hardware description languages and test their logic behaviour

MO3 Apply quantitative methods and integrated development tools relevant to the design of digital electronic systems

MO4 Demonstrate ability in the use of oscilloscopes, logic analysers and programmable devices

Hours to be allocated: 150

Contact hours:

Independent study/self-guided study = 114 hours

Laboratory work = 24 hours

Total = 150

Reading list: The reading list for this module can be accessed at readinglists.uwe.ac.uk via the following link https://uwe.rl.talis.com/modules/ufmfqt-15-2.html

Part 4: Assessment

Assessment strategy: In this module students individually develop the technical skills to design, simulate, analyse and verify a complex digital system through a collaborative learning strategy with the aid of a set of structured laboratory exercises. This will extend the students understanding of the tools and techniques required to become an expert in digital system design.

Component B consists of a portfolio of regular laboratory exercises with reflections that builds confidence and ensures students are prepared for a controlled-conditions, practical assessment at the end of the module.

Component A will involve an end of module individual practical examination involving computer based and lab-based practical aspects of digital electronic design.

Resit strategy
Component B coursework submission will be an individual report of an digital electronic design exercise that encompasses critical aspects of learning expected through the laboratory work.
Component A will be an individual examination as described in the first sit assessment.

Assessment components:

Examination - Component A (First Sit)
Description: Laboratory based examination (2 hours)
Weighting: 50 %
Final assessment: Yes
Group work: No
Learning outcomes tested: MO1, MO2, MO3, MO4

Portfolio - Component B (First Sit)
Description: Laboratory reports and reflection
Weighting: 50 %
Final assessment: No
Group work: No
Learning outcomes tested: MO1, MO2, MO3, MO4

Examination - Component A (Resit)
Description: Laboratory based exam (2 hours)
Weighting: 50 %
Final assessment: Yes
Group work: No
Learning outcomes tested: MO1, MO2, MO3, MO4

Report - Component B (Resit)
Description: Report of individual design exercise (1500 words)
Weighting: 50 %

Final assessment: No

Group work: No

Learning outcomes tested: MO1, MO2, MO3, MO4

Part 5: Contributes towards

This module contributes towards the following programmes of study:

Electronic and Computer Engineering [Sep][FT][Frenchay][3yrs] BEng (Hons) 2020-21

Electronic Engineering [Sep][SW][Frenchay][4yrs] BEng (Hons) 2020-21

Electronic Engineering [Sep][FT][Frenchay][3yrs] BEng (Hons) 2020-21

Electronic and Computer Engineering [Sep][SW][Frenchay][4yrs] BEng (Hons) 2020-21

Electronic and Computer Engineering [Sep][PT][GlosColl][5yrs] BEng (Hons) 2020-21

Electronic and Computer Engineering {Apprenticeship-GLOSCOLL} [Sep][FT][GlosColl][5yrs] BEng (Hons) 2020-21