Module Specification

System Design Using HDLs

Version: 2023-24, v4.0, 28 Jun 2023

Contents

Part 1: Information

Module title: System Design Using HDLs

Module code: UFME7G-15-M

Level: Level 7

For implementation from: 2023-24

UWE credit rating: 15

ECTS credit rating: 7.5

College: College of Arts, Technology and Environment

School: CATE School of Engineering

Partner institutions: None

Field: Engineering, Design and Mathematics

Module type: Module

Pre-requisites: None

Excluded combinations: None

Co-requisites: None

Continuing professional development: No

Professional, statutory or regulatory body requirements: None

Part 2: Description

Overview: Not applicable

Features: Not applicable

Educational aims: See Learning Outcomes.

Outline syllabus: Comparison with other HDLs
Role of VHDL in hardware-software co-design
Simulation and Verification

Design for synthesis and re-use

FPGAs as target hardware

System-on-chip design tools and techniques

Safety standards for hardware systems, eg IEC61508

Part 3: Teaching and learning methods

Teaching and learning methods: Scheduled Learning in the form of lectures, tutorials, demonstrations and independent learning laboratory work.

Independent Learning will include directed reading, tutorial exercises, general reading of trade journals, academic papers and other texts.

Module Learning outcomes: On successful completion of this module students will achieve the following learning outcomes.

MO1 Demonstrate the appropriate use of verification and debug tools and techniques

MO2 Make an evaluation of the commercial risks of developing a new system

MO3 Demonstrate the application of engineering techniques within commercial constraints

MO4 Show understanding of the need to apply a systems approach to engineering problems and why engineers have to work with uncertainty

MO5 Demonstrate the ability to develop an innovative design for a new system

Hours to be allocated: 150

Contact hours:

Independent study/self-guided study = 126 hours

Face-to-face learning = 24 hours

Total = 150

Reading list: The reading list for this module can be accessed at readinglists.uwe.ac.uk via the following link https://uwe.rl.talis.com/modules/ufme7g-15-m.html

Part 4: Assessment

Assessment strategy: The module will be assessed as follows:

An examination will assess the student's ability to develop a solution to a design specification along with their understanding of the design principles necessary.

Demonstration of an innovative solution to a design problem along with submission of a report or log book.

Formative feedback will be provided during the laboratory sessions and tutorials.

Resit is the same as the first sit

Assessment tasks:

Portfolio (First Sit)
Description: Logbook showing development process and demostration of final product
Weighting: 75 %
Final assessment: No
Group work: No
Learning outcomes tested: MO1, MO2, MO3, MO5

Examination (Online) (First Sit)
Description: Examination (2 hours + 2 hours for submission)
Weighting: 25 %
Final assessment: Yes
Group work: No

Learning outcomes tested: MO4

Portfolio (Resit)
Description: Logbook showing development process and demostration of final product
Weighting: 75 %
Final assessment: No
Group work: No
Learning outcomes tested:

Examination (Online) (Resit)
Description: Examination (2 hours + 2 hours for submission)
Weighting: 25 %
Final assessment: Yes
Group work: No
Learning outcomes tested:

Part 5: Contributes towards

This module contributes towards the following programmes of study:

Digital Electronic Systems Engineering {Apprenticeship-UWE} [Frenchay] - Suspended MSc 2023-24

Electronic Engineering [Sep][FT][Frenchay][4yrs] MEng 2020-21

Electronic Engineering [Sep][SW][Frenchay][5yrs] MEng 2019-20