STUDENT AND ACADEMIC SERVICES

**MODULE SPECIFICATION**

| Part 1:  Information | | | |
|---|---|---|---|
| Module Title | System Design Using HDLs | | |
| Module Code | UFME7G-15-M | Level | Level 7 |
| For implementation from | 2019-20 | | |
| UWE Credit Rating | 15 | ECTS Credit Rating | 7.5 |
| Faculty | Faculty of Environment & Technology | Field | Engineering, Design and Mathematics |
| Department | FET Dept of Engin Design & Mathematics | | |
| Module type: | Standard | | |
| Pre-requisites | None | | |
| Excluded Combinations | None | | |
| Co- requisites | None | | |
| Module Entry requirements | None | | |


| Part 2: Description |
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**Educational Aims:** See Learning Outcomes.

**Outline Syllabus:** Comparison with other HDLs
Role of VHDL in hardware-software co-design
Simulation and Verification
Design for synthesis and re-use
FPGAs as target hardware
System-on-chip design tools and techniques
Safety standards for hardware systems, eg IEC61508

**Teaching and Learning Methods:** Scheduled Learning in the form of lectures, tutorials, demonstrations and independent learning laboratory work.

Independent Learning will include directed reading, tutorial exercises, general reading of trade journals, academic papers and other texts.

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| Part 3: Assessment | |
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The module will be assessed in two components.

(Component A) By laboratory examination. The examination will assess the student's ability to develop a solution to a design specification along with their understanding of the design principles necessary.

(Component B) Demonstration of an innovative solution to a design problem along with submission of a report or log book.

Formative feedback will be provided during the laboratory sessions and tutorials.

| First Sit  Components | Final Assessment | Element weighting | Description |
|---|---|---|---|
| Portfolio - Component B | | 75 % | Logbook showing development process and demostration of final product |
| Examination - Component A | ✓ | 25 % | Laboratory examination (3 hours) |
| Resit  Components | Final Assessment | Element weighting | Description |
| Portfolio - Component B | | 75 % | Design exercise and demonstration |
| Examination - Component A | ✓ | 25 % | Laboratory examination (3 hours) |

| Part 4:  Teaching and Learning Methods | |
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| Learning Outcomes | On successful completion of this module students will achieve the following learning outcomes: |
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| Module Learning Outcomes | Reference |
|---|---|
| Demonstrate the appropriate use of verification and debug tools and techniques | MO1 |
| Make an evaluation of the commercial risks of developing a new system | MO2 |
| Demonstrate the application of engineering techniques within commercial constraints | MO3 |
| Show understanding of the need to apply a systems approach to engineering problems and why engineers have to work with uncertainty | MO4 |
| Demonstrate the ability to develop an innovative design for a new system | MO5 |

| Contact Hours | **Independent Study Hours:** | |
|---|---|---|
| | Independent study/self-guided study | 126 |
| | **Total Independent Study Hours:** | 126 |
| | **Scheduled Learning and Teaching Hours:** | |
| | Face-to-face learning | 24 |

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|---|---|---|---|
| | **Total Scheduled Learning and Teaching Hours:** | 24 | |
| | | 3 | |
| | **Hours to be allocated** | 150 | |
| | **Allocated Hours** | 150 | |
| Reading List | *The reading list for this module can be accessed via the following link:*<br><br>https://uwe.rl.talis.com/modules/ufme7g-15-m.html | | |

| **Part 5:  Contributes Towards** |
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| This module contributes towards the following programmes of study: |